PPM-2030C

Mini 80386SX
20MHz Mainboard
User's Manual

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Edition 1.01

Warning

Reconfiguring

NEVER reconfigure the board while the power is ON.

If you wish to reconfigure the board at any time, make sure that the power is turned OFF before changing any hardware settings such as DIP switches or jumpers.

Note

- When you see an error message on the screen after turning the power on, leave the system switched on for one to two hours to charge the battery. You can then enter the system configuration.
- Later, leave your system switched on for 10 to 15 hours to completely charge the battery.
- If you leave the system switched off for more than one month, repeat the steps above.
- If you are using an onboard battery, be sure **pins BATT and INT (2 and 3) of jumper W13 are shorted** when you install your system. Otherwise, you will have to set up your configuration whenever you turn on your computer.

Checklist

Your PPM-2030C mainboard package contains the following:

- One PPM-2030C mainboard
- One user's manual
- One BIOS system setup manual
- One EMS driver diskette

Contents

Introduction

The PPM-2030C mainboard is compatible with the PC/AT. This means that virtually all the software available for the PC/AT can also be run on a system you build around the PPM-2030C mainboard.

The PPM-2030C incorporates the Intel 80386SX which is a 32-bit CPU with a 16-bit external data bus and a 24-bit external address bus. The 80386SX CPU brings the high-performance software of the Intel 80386 architecture to midrange systems. It provides the performance benefits of a 32-bit programming architecture and the cost savings associated with 16-bit hardware systems.

Moreover, the 80386SX microprocessor is 100% object-code compatible with the 386, 286, and 8086 microprocessors. Therefore, PPM-2030C CPU-based systems optimize both for performance and cost. The PPM-2030C can access the world's largest existing microcomputer software base, including the growing collection of 32-bit software.

For these reasons, the PPM-2030C mainboard is the ideal choice for a person seeking affordable '386 power.

The clear, well-illustrated instructions in this manual ensure that even if you are a newcomer to the computer world, you will have your system installed and running with a minimum of effort.

The PPM-2030C includes the following features:

- Intel 80386SX-20 microprocessor — 32-bit CPU with a 16-bit external data bus and a 24-bit external address bus
- Intel 80387SX-20 coprocessors optional
- Use of C&T's CS8221 PC/AT-compatible chip set.
- Switchable between 10MHz Normal mode and 20MHz Turbo mode by either a software switch or a hardware switch
- Onboard battery backup for CMOS configuration table and real-time clock
- RAM subsystem of 512KB, 640KB, 1MB, 1.5MB, 2MB, 3MB, 4MB and 5MB
- Eight expansion slots — Six 16 bit slots and two 8 bit slots
- Sixteen-level interrupt
- Seven-channel DMA for disk and special I/O
- 64KB legal DTK BIOS (ADL certified) developed by Datatech Enterprises Co., Ltd.
- Four-layer mainboard
- LIM 4.0 EMS support
- Shadow RAM support
- Choice of either 44256 DIP or 256K/1M SIMM DRAM modules with 80ns
- Page/Interleaved DRAM access method support
- Power fail detect circuit
- Address pipeline support

Board Layout

Below is a layout of the PPM-2030C showing the jumpers and some of the connectors. The figure on the next page gives the dimensions of the board.

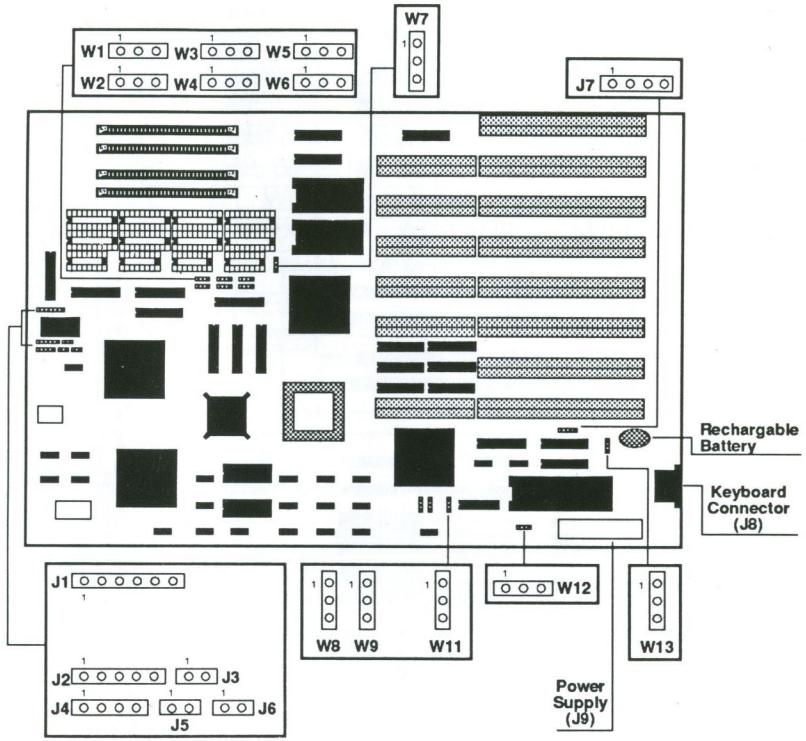
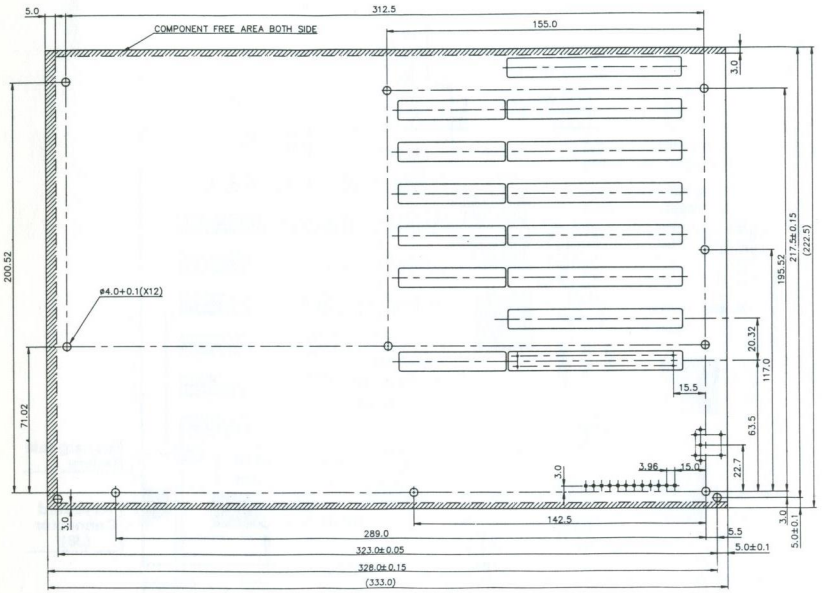


Figure: The Location of Jumpers and Connectors

Dimensions of PPM-2030C

All the dimensions are in millimeter(s).



Board Setup

In this section references will be made to jumper settings used to configure the various functions of the PPM-2030C mainboard. Refer to the Board Layout section for locations of all jumpers.

RAM Installation

Jumpers W1- W6 are used to set the RAM size you want on the mainboard. The DIP and SIMM DRAM banks can contain from 512KB, 640KB, 1MB, 1.5MB, 2MB, 3MB, 4MB to 5MB by means of setting jumpers W1 - W6. Refer to the illustration below for the location of jumpers W1 - W6 and the RAM banks.

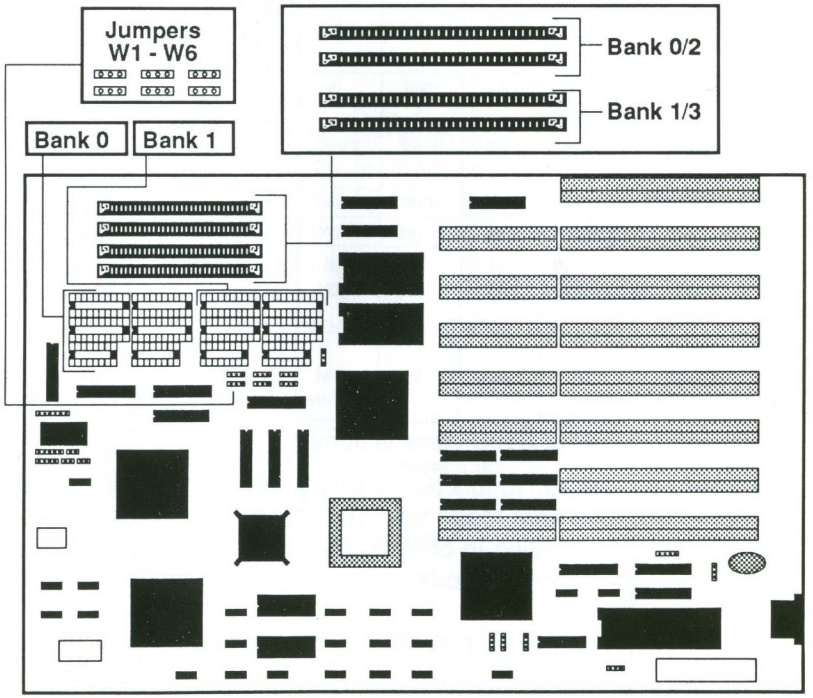


Figure: RAM Banks & Jumpers for Bank Selection

The following figures show the configuration for total onboard system memory.

Description	W1 - W6 Settings
Using one bank or two banks (banks 0 & 1) with either DIP or SIMM DRAMs as onboard memory	
Using three or four banks of DIP (banks 0, 1) and SIMM (banks 2, 3) DRAMs as onboard memory	

Total System Memory	DRAM Type				Wait-State	Page Interleave	Reference
	Bank 0	Bank 1	Bank 2	Bank 3			
512K	256K	0K	0K	0K	1	Disable	Page 8
640K	256K	64K	0K	0K	1	Disable	Page 9
1MB	256K	256K	0K	0K	0	Enable	Page 10
					1	Enable	
					1	Disable	
1.5MB	256K	256K	256K	0K	1	Disable	Page 11
2MB	256K	256K	256K	256K	0	Enable	Page 12
					1	Enable	
					1	Disable	
2MB	1M	0K	0K	0K	1	Disable	Page 12
3MB	256K	256K	1M	0K	1	Disable	Page 13
4MB	1M	1M	0K	0K	0	Enable	Page 14
					1	Enable	
					1	Disable	
5MB	256K	256K	1M	1M	0	Enable	Page 15
					1	Enable	
					1	Disable	

RAM access time is 80ns

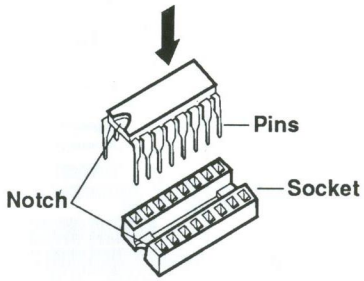
Note: To function normally, your system has to be in **Normal Mode** but not Turbo mode, if your system is operating in both zero wait-state and disabled page interleave mode.

Million Instruction Per Second Test

The Million Instruction Per Second (MIPS) performance test — for page-interleave/zero-wait is in 2.45 and for Turbo mode/one-wait is 2.23.

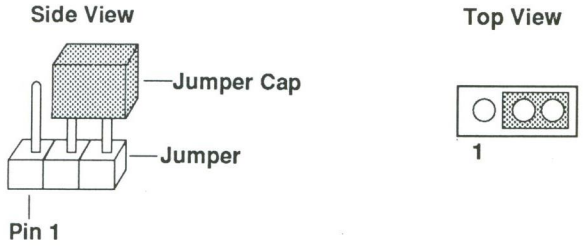
Chip Insertion

Remember that when inserting chips, you must make sure the notched or dotted end of the chip is lined up with the notched end of the socket. Gently push the chip into the socket, and be careful not to bend the pins.



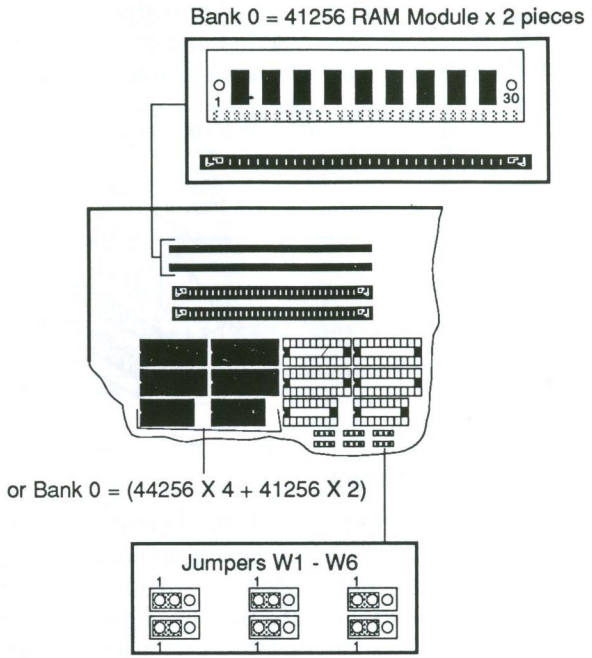
Jumper

A jumper is a kind of switch which uses a plastic cap with a metal interior to connect (short) two pins. If a jumper needs to be left open, you should save the cap for future use by covering one pin only of the jumper. This has no effect on the function of the board while it keeps the cap handy. The illustration below shows the side and top views of a three-pin jumper in which pins two and three are shorted.



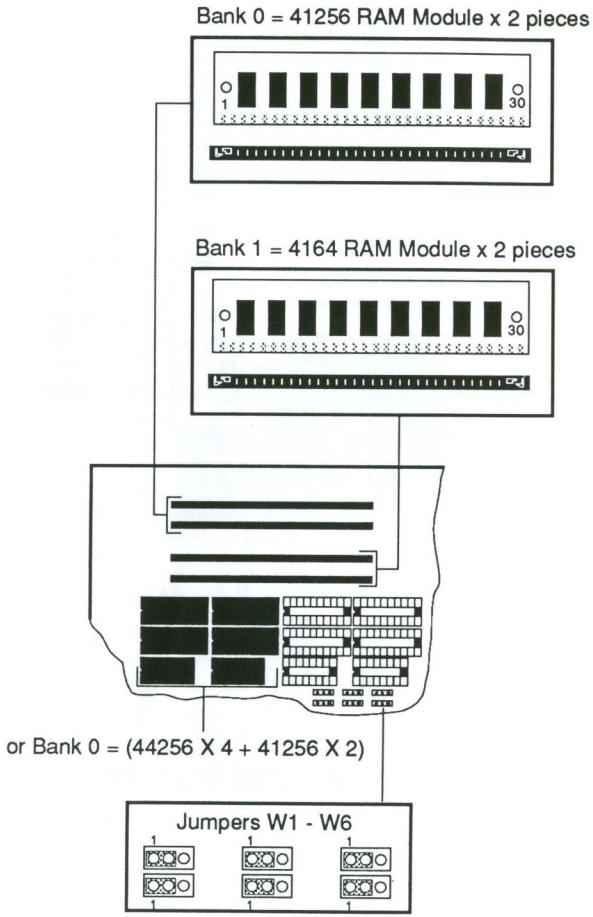
To select the proper jumper setting for the RAM size that you want, refer to the figures on the following pages.

512KB Total Onboard System Memory



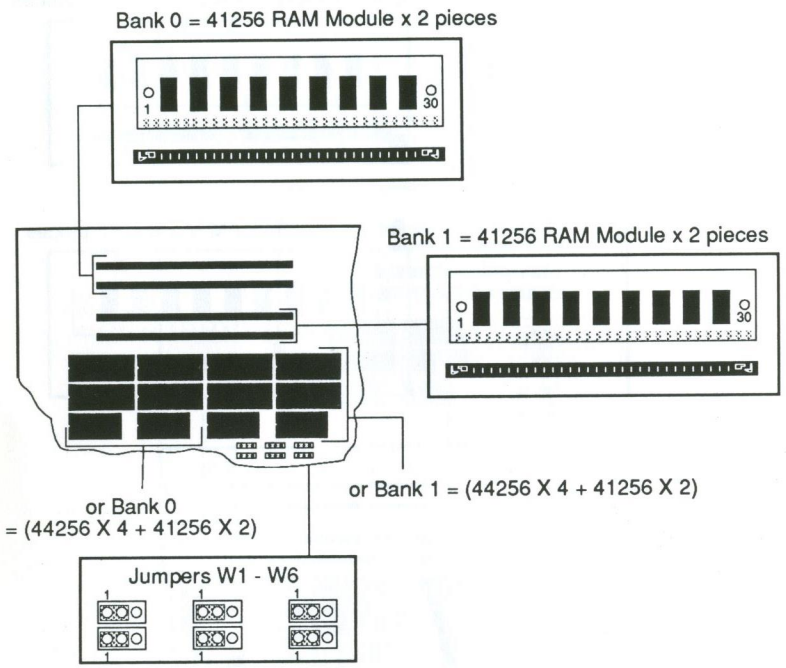
You may use either bank as bank 0.

640KB Total Onboard System Memory



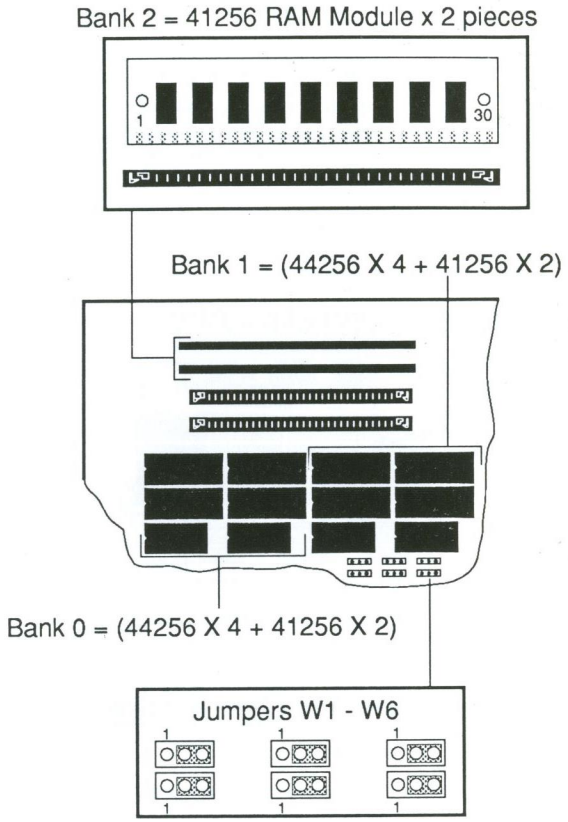
You may use either bank as bank 0.

1MB Total Onboard System Memory

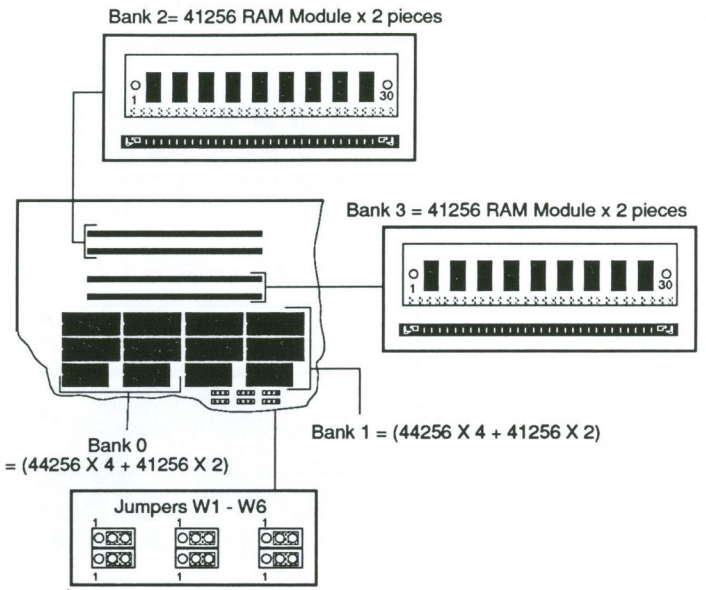


Any bank 0 may be used with any bank 1.

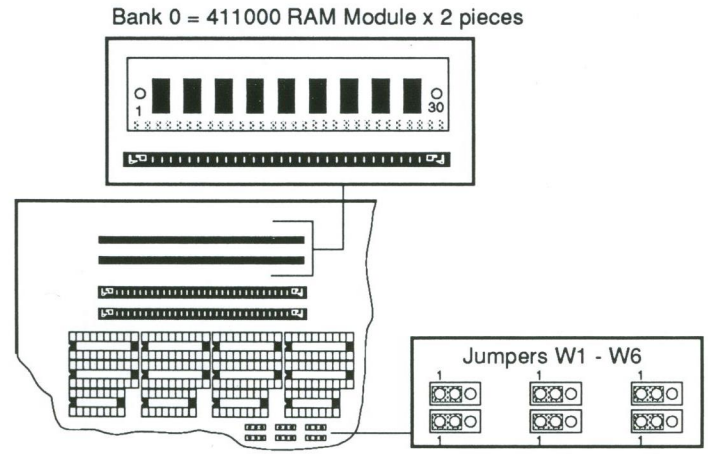
1.5MB Total Onboard System Memory



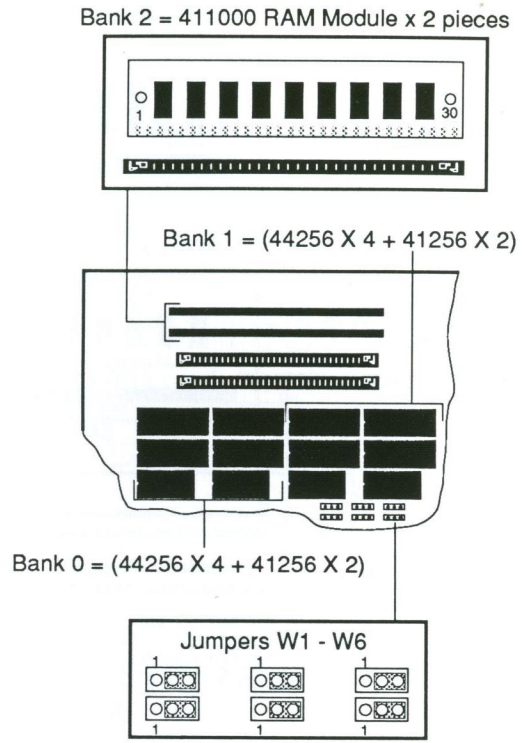
2MB Total Onboard System Memory



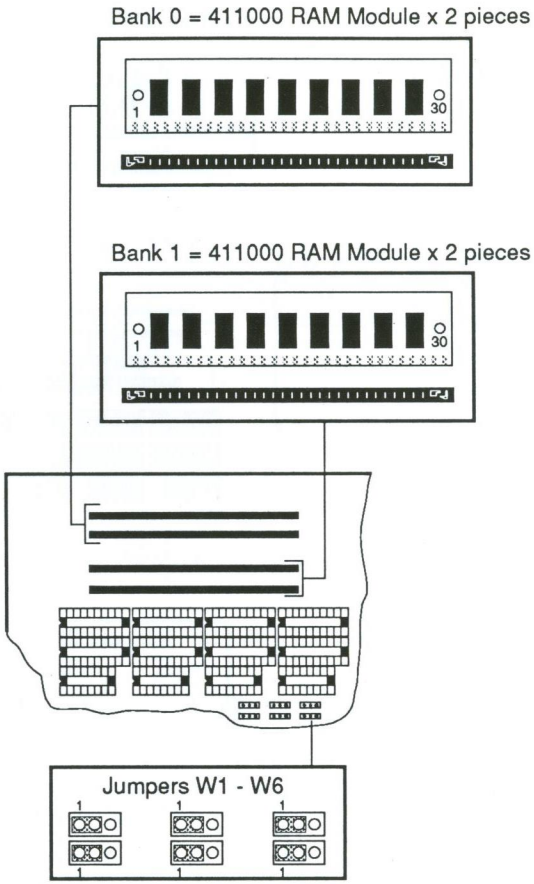
2MB Total Onboard System Memory



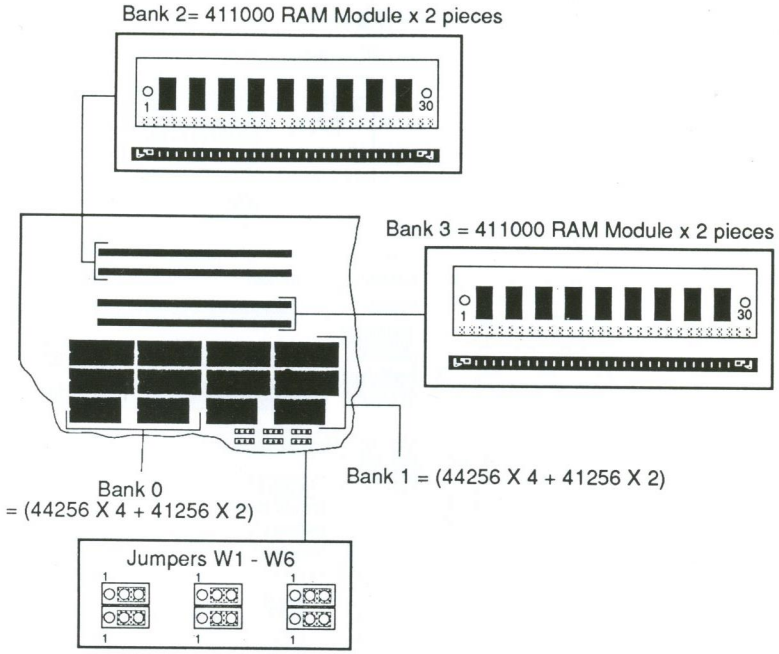
3MB Total Onboard System Memory



4MB Total Onboard System Memory



5MB Total Onboard System Memory



ROM Installation

To install the ROM chips, refer to the illustration below for the location of the chip sockets and ROM selection jumper W7 on the mainboard.

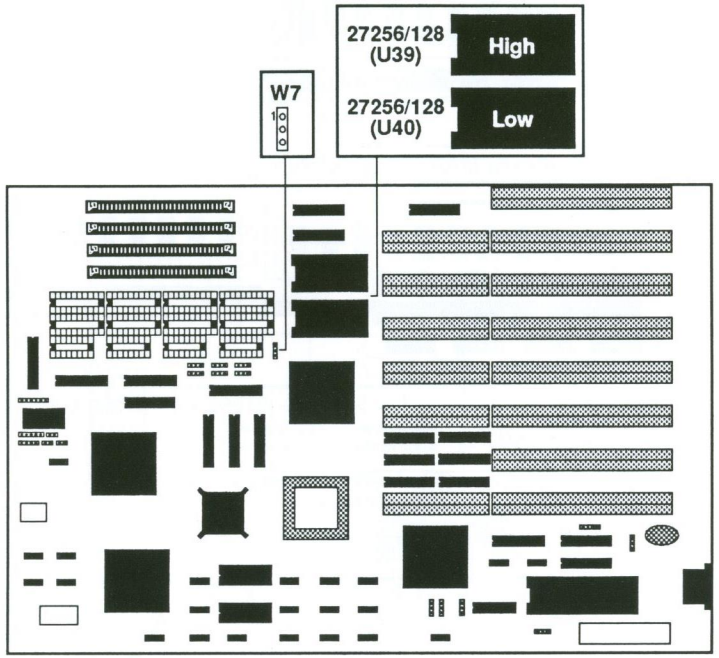


Figure: Installing ROM

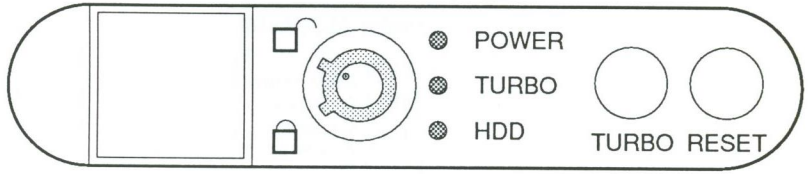
Type of BIOS	Type of ROM chip	ROM Configuration	Jumper W7
DTK BIOS or any other of 64KB size	27256 x 2	U39 - High byte U40 - Low byte	1
Other BIOS of 32KB size	27128 x 2	U39 - High byte U40 - Low byte	1

ROM access time is 200ns.

Table: Type of BIOS

Connectors

A variety of connections can be made from the PPM-2030C mainboard to a control panel on the front of your system. In addition you can connect a speaker (which comes installed in most system unit cases). There are a variety of different control panel designs currently available with system unit cases. Ideally the control panel will include a keyboard lock, a reset switch, a microprocessor speed switch with a LED (commonly referred to as a Turbo switch) and LEDs that indicate power and hard disk activity. The panel will probably look something like the figure below.



Functions of Panel Indicators and Switches

Following is a brief explanation of the various functions of a control panel that the PPM-2030C supports:

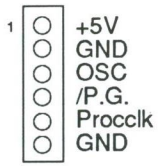
CPU Frequency Indicator (Jumper J1)

The CPU frequency indicator is used to indicate the speed of the 80386SX CPU. The PPM-2030C is switchable between 10 and 20MHz.

Make sure pin one of the connector for the CPU frequenccy indicator on the control panel matches pin one of jumper J1. Otherwise, you will destroy the display LED.

Refer to the figure on the following page for the pinout.

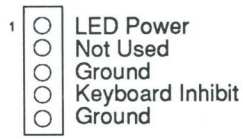
Jumper J1 Pinouts



Keylock & Power LED (Jumper J2)

Jumper J2 is used to enable the use of the keyboard and the power LED. By disabling the keylock, you can "lock" the data in your computer. Unlocking the keylock enables the keyboard. Refer to the table below for its pinouts.

Jumper J2 Pinouts



Hardware Switch (Jumper J3)

The hardware switch (Turbo switch) allows you to toggle the speed between 10MHz and 20MHz. Refer to the figures below for the pinouts and jumper settings.

Jumper J3	Hardware Switch
	Turbo
	Normal

Jumper J3 Pinouts

Speaker (Jumper J4)

Jumper J4 is used to connect a speaker. When the four pins are connected to a speaker in a closed circuit, the speaker is functional. Refer to the figure below for the pinouts.

Jumper J4 Pinouts

Turbo LED (Jumper J5)

Jumper J5 is used to enable Turbo LED. The Turbo LED in the hardware switch indicates operation in the Turbo mode.

Jumper J5 Pinouts

Reset (Jumper J6)

Jumper J6 is used to enable the hardware reset. If you encounter any problems while using unfamiliar software, you can always restart from the beginning by pressing the reset button. Note, however that any data which have not been saved to disk will be lost. Refer to the figure below for its pinouts.

Jumper J6 Pinouts

Display Adapter Settings

Jumper W12 is used to select the display adapter. Refer to the Board Layout section for the location of W12. To configure the mainboard for the kind of display adapter you want, set jumper W12 according to the table below.

Jumper W12	Video Selection
	Monochrome
	Color

Power Good and Power Fail Detect

The PPM-2030C provides power fail detect and external "power-good" signals to indicate proper operation of the power supply. Jumper W11 is used to select an onboard or external power-good signal.

When the power supply is unstable or the power-good signal does not work well, the external power-good will still operate at minimum line voltage and maximum load, but data loss may occurred. And you are advised to use the power fail detect function (pins one and two of jumper W11 shorted).

Jumper W11	Function
	Power Fail Detect Circuit Active
	External Power-Good Function Active

80386SX CPU

The PPM-2030C uses an Intel 80386SX-20 microprocessor running at 20MHz. The 80386SX has a number of features that enable a substantial leap in processing power and capability over the 80286 standard used in AT-type microcomputers. Aside from being able to execute 80286 programs, the 80386SX is capable of concurrent processing, hardware-based multi-tasking and the creation of 8086 "virtual machines". The 80386SX has superior extended memory support and will execute the new 32-bit programs of the future.

Address Pipeline

Jumper W8 is used to enable or disable piplining. If piplining is enabled, the processor can access data more quickly.

Refer to the figure below for the jumper settings and pinouts.

Jumper W8	Pipelining
	Disabled
	Enabled

Jumper W8 Pinouts

An optional 80387SX-20 coprocessor can be installed in socket U42 to accelerate calculation-intensive applications.

Jumper W9 is used to enable or disable the 80387SX coprocessor.

Make sure the notched of the 80387SX is lined up with the notched end of the socket.

Refer to the figures below and on the next page for jumper W9, the 80386SX and 80387SX.

Jumper W9	80387SX
1 	Enable
1 	Disable

Table: 80387SX Selection

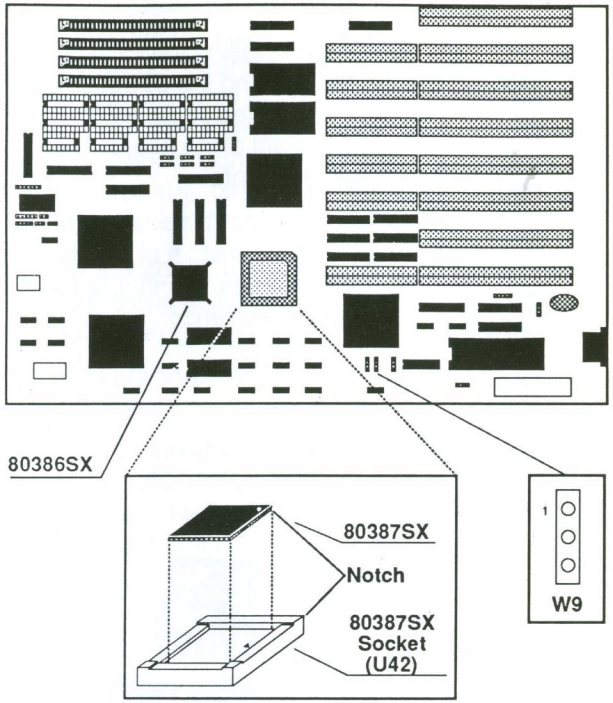
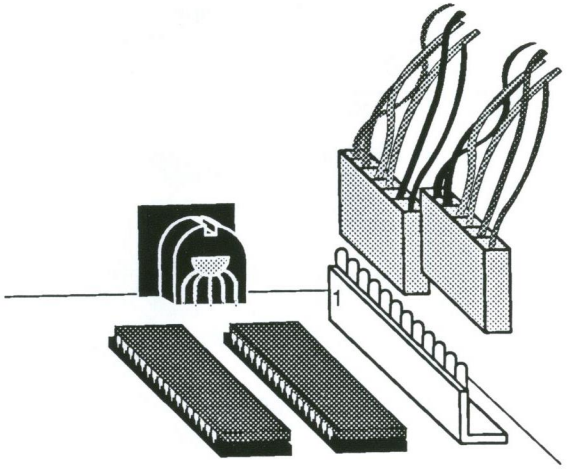


Figure: The location of W9, 80386SX and 80387SX

Connection to Power Supply

If you are installing the PPM-2030C yourself, the final step is attaching the power supply cable to the main-board at connector J9, which is located in the upper right quadrant of the board. There are some cables on the power supply.

Be sure the four black wires of the power supply are located at the middle of the power connectors. Refer to the figure below. Pin 1 is numbered in the picture for your convenience.



The pinouts for the connectors at J9 are as follows:

Pin	Assignment
1	Power Good
2	+5 VDC
3	+12 VDC
4	-12 VDC
5	Ground
6	Ground
7	Ground
8	Ground
9	-5 VDC
10	+5 VDC
11	+5 VDC
12	+5 VDC

Choosing a Power Supply

The power supply provides a "power-good" signal to indicate proper operation of the power supply. The power-good signal is a TTL-compatible high level for normal operation or a low level for fault conditions. If the power-good signal works well, the system will function properly. Otherwise, the CMOS RAM data setting will be lost.

You are advised to use the internal power fail detect circuit (pins one and two of jumper W11 shorted) if the external power-good signal does not work well.

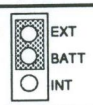
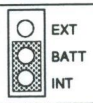
Following are some guidelines for choosing a suitable power supply:

- The power-good signal should have a turn-on delay of at least 200ms, but no longer than 500ms. (This means that the power-good signal goes to a high level later than +5V).
- The power-good signal goes to a low level at least 100ms before +5V falls below the regulation limits when the power is turned off.

To install a power supply in your system case you may need to consult your dealer for information. Nevertheless, installation is a simple and straightforward procedure.

Battery Connector

Jumper W13 is used to select an external battery or the onboard rechargable battery. Refer to the Board Layout section for the location of W13. Jumper J7 is enables four size "AA" batteries instead of the circular lithium battery to power the CMOS RAM. Refer to the figures below.

Jumper W13	Battery
	External
	Onboard

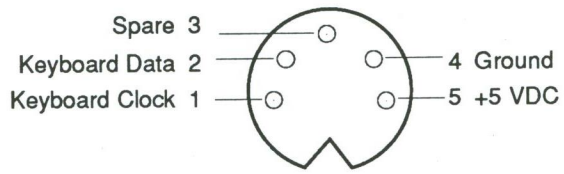
Jumper J7 Pinouts

Be sure pins 2 and 3 of jumper W13 are shorted when you install your system. Otherwise, you will have to set up your system configuration whenever you turn on your computer.

Keyboard Connector (J8)

The keyboard connector may be located at the back of your system unit. The pin assignments for keyboard connector J8 are as follows:

Jumper J8 Pinouts



Software

PPM-2030C supports shadow RAM and Expanded Memory System (EMS) to increas the system memory capability.

Note that If you have more than one megabyte memory, you may enable or disable the 384K memory as shadow RAM.The 384K is always allocated at the same address for shadow RAM, even if you disable the shadow RAM.

IMPORTANT: You can only enter the setup menu by pressing <Esc> when the power is switched on. You may reset the system to enter setup menu, too.

Shadow RAM Enable

For efficient execution of BIOS, it is preferable to run BIOS code through RAM rather than through the slower EPROMs. The PPM-2030C can support shadow RAM for BIOS and video.

To enable shadow RAM, follow the steps below:

- Hold down the <Esc> key to enter the DTK setup menu as you turn the power on.
- Select item 6 to enter CHIP setup
- Select item 1 to enable BIOS or video shadow RAM (Refer to the DTK BIOS manual for details.)

EMS Driver Setup

The PPM-2030C mainboard support LIM 4.0 EMS. To set up the EMS driver, follow the steps below:

- Hold down the <Esc> key to enter the DTK BIOS setup program. Choose item 6 to enter the CHIP setup menu. From this menu, you may enable EMS and select EMS size. (Refer to the DTK BIOS manual for details.)

NOTE: If you only have one megabyte onboard memory, you must disable the shadow RAM function first in order to use 384K extended memory as expanded memory.

- Insert the EMS driver diskette into drive A and enter a: .
- Enter this command:

  INSTALL

  You will see the following screen.

```
This program installs the NEAT EMS driver on your hard disk.
(Press Esc key to quit: any other key to continue installation)
```

- The next screen will be as below if you continue setup.

```
Enter the path name for the location of NEMM.SYS:
C:\NEMS
(Press Esc key to quit: any other key to continue installation)
```

Indicate the path name where NEMM.SYS is to be located. If you want the program to create a directory with the default name (NEMS) on your hard drive, press the Enter key. Otherwise, type in the path and directory name of your choice.

- A screen like the following will appear:

```
        DTK NEAT EMS hardware configuration setup.
        Select the option you want for each item

PAGE REGISTER I/O : 0          0: 208H/209H
BASE ADDRESS                   1: 218H/219H
                               2: 258H/259H
FRAME START ADDRESS:4          3: 268H/269H
                               4: 2A8H/2A9H
                               5: 2B8H/2B9H
                               6: 2E8H/2E9H
F1:accept,Esc, ↑ ↓
```


Indicate two parameters for EMS — page register I/O base address and frame start address.

- Choose the correct configuration as you desire, then press <F1> to complete setup.

You will get a warning if you give an incorrect response. For example, if you give D000H as your frame start segment, and shadow RAM in the same area, the following message will appear.

```
        DTK NEAT EMS hardware configuration setup.
        Select the option you want for each item

PAGE REGISTER I/O : 0          0: C000H, C400H, C800H, CC00H
BASE ADDRESS                   1: C400H, C800H, CC00H, D000H
                               2: C800H, CC00H, D000H, D400H
FRAME START ADDRESS:4          3: CC00H, D000H, D400H, D800H
                               4: D000H, D400H, D800H, DC00H
                               5: D400H, D800H, DC00H, E000H
                               6: D800H, DC00H, E000H, E400H
                               7: DC00H, E000H, E400H, E800H
F1:accept,Esc, ↑ ↓             8: E000H, E400H, E800H, EC00H

Cannot use as frame! This address is allocated for
Shadow RAM or ROM enable!
```

- If the installation is complete, the following will appear:

```
The installation is complete. Remove the diskette and
press Ctrl+Alt+Del to restart the system.
```

- Reboot your system. The screen will look like this:

```
================================================================
DTK NEAT Expanded Memory Manager Ver. 1.00 1989
(C) Copyright Datatech Enterprise Co.,Ltd
All Rights Reserved
================================================================

       User specified PAGE PORT = 208H
       User specified PAGE FRAME = D000H
       Test Expanded Memory Page 128
       There are 128 PAGEs for EMS.
       NEMM.SYS has been installed.
```

Operation

The main advantage of the PPM-2030C 20MHz mini-80386SX mainboard over ordinary PC/AT mainboards is its dual clock system. This innovation makes it possible for your computer to operate at either of two clock speeds: 10MHz or 20MHz.

Entering 20MHz Turbo Mode

The PPM-2030C supports both a software and hardware switch to toggle between 10MHz and 20MHz (Turbo) modes. The two switches are set up using jumper J3 and are mutually exclusive. You must choose either software or hardware if you are setting up the board yourself.

Software Turbo Switch

When jumper J3 is covered with a jumper cap or is connected to a closed hardware Turbo switch, the speed can be toggled between Turbo and Normal from the keyboard. The clock speed when you turn the system on will be 10MHz (or 20MHz). To switch the speed to 20MHz (or 10MHz), do the following: press and hold down the control <Ctrl> and alternate <Alt> keys on the keyboard while you press the minus <-> key. The Turbo LED on your panel, if you have one, will light. For more information on the Turbo LED, refer to the Connectors section.

Hardware Turbo Switch

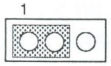
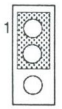
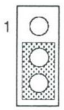
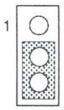
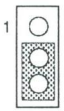
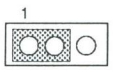
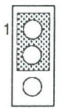
If your hardware Turbo switch is connected to pins one and two of jumper J3, pushing the switch on and off will toggle between 10MHz Normal mode and 20MHz Turbo mode.

Alternate Use of Both Switches

Both the hardware and the software switches may be used alternatively, but this is not advised because you may become confused about the mode of operation. When using both switches alternatively, the Turbo LED will be the only accurate indicator of the actual mode: the LED will be on in Turbo mode and off in Normal mode.

Default Settings

Because of the number of jumpers and options on the board, it is recommended to start with the default settings, and make experimental modifications from that point. The following table shows the default settings.

Jumpers	Function
W1 - W6 	Used One or Two Banks Only
W7 	27256 ROM
W8 	Pipeline Enabled
W9 	80387SX Disabled
W11 	External Power-Good
W12 	Mono Display
W13 	External Battery

Technical Information

Microprocessor

The 80386SX is a high-performance microprocessor with a 16-bit external data path, up to 16 megabytes of directly addressable physical memory and up to 64 terabytes of virtual memory space. The operating speed of the 80386SX chip is 10MHz in Normal mode and 20MHz in Turbo mode.

The 80386SX operates in two modes: protected virtual address mode and real address mode.

Protected Virtual Address Mode

In protected mode, software can perform a task switch to enter virtual 8086 mode tasks. Each task behaves with 8086 semantics, thus allowing 8086 software (an application program or an entire operation system) to execute. The virtual 8086 tasks can be isolated and protected from one another and the host 386SX microprocessor operation system by use of paging.

Protected mode will use one of two different address spaces, depending on whether or not paging is enabled. Every selector has a logical base address of up to 32 bits in length. This 32-bit logical base address is added to the effective address to form a final 32-bit linear address. If paging is disabled, this final linear address reflects physical memory and is truncated so that only the lower 24 bits of this address are used to address the 16 megabyte memory address space. If paging is enabled this final linear address reflects a 32-bit address. This is translated through the paging unit to form a 16-megabyte physical address.

Real Address Mode

In real mode the 386SX microprocessor operates as a very fast 8086, but with a 32-bit extension if desired. Real mode is required primarily to set up the processor for protected mode operation.

The segmentation unit shifts the selector left four bits and adds the result to the effective address to form the linear address. This linear address is limited to 1 megabyte. In addition, real mode has no paging capability.

System Timers

The system has three programmable timer/counters controlled by the Intel 8254-2 chip. These are channels 0 through 2 defined as follows:

Channel 0	System Timer
GATE 0	TIED ON
CLK IN 0	1.190MHz OSC
CLK OUT 0	8259A IRQ 0

Channel 1	Refresh Request Generator
GATE 1	TIED ON
CLK IN 1	1.190MHz OSC
CLK OUT 1	Request Refresh Cycle

NOTE: Channel 1 is programmed to generate a 15 microsecond signal.

Channel 2	Tone Generation for Speaker
GATE 2	Controlled by bit 0 of port hex 61 PP1 bit
CLK IN 2	1.190MHz OSC
CLK OUT 2	Used to drive speaker

The 8254-2 timer/counter is treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters; the fourth is a control register for mode programming.

System Interrupts

Sixteen levels of system interrupts are provided by the 80386SX NMI and two 8259A interrupt controller chips. The following shows the interrupt-level assignments' decreasing priority:

Level	Function
Microprocessor NMI	Parity or I/O Channel Check
Interrupt Controllers	
CTLR1 CTLR2	
IRQ 0	Timer Output 0
IRQ 1	Keyboard (Output Buffer Full)
IRQ 2 ◄	Interrupt from CTLR 2
IRQ 8	Realtime Clock Interrupt
IRQ 9	Software Redirected to INT OAH (IRQ2)
IRQ 10	Reserved
IRQ 11	Reserved
IRQ 12	Reserved
IRQ 13	Coprocessor
IRQ 14	Fixed Disk Controller
IRQ 15	Reserved
IRQ 3	Serial Port 2
IRQ 4	Serial Port 1
IRQ 5	Parallel Port 2
IRQ 6	Diskette Controller
IRQ 7	Parallel Port 1

ROM Subsystem

The ROM subsystem has a 32K by 16-bit arrangement consisting of two 32K by 8-bit ROM/EPROM modules. The odd and even address codes reside in separate modules. The top of the first megabyte and the bottom of the last megabyte address space is assigned to ROM (hex 0F0000 and hex FF0000). Parity checking is not done on ROM.

DTK BIOS has been provided in this subsystem.

RAM Subsystem

The RAM subsystem starts at address hex 000000 of the 16M address space. It consists of either 640KB or 1MB in the form of 256K or 64K by 1-bit RAM modules. Memory refresh forces one memory cycle every 15 microseconds through channel 1 of the timer/counter. The following functions are performed by the RAM initialization program:

- Write operation to any memory location.
- Initialization of channel 1 of the timer/counter to the rate generation mode (15 microseconds).

NOTE: Memory can be used only after being accessed or refreshed eight times.

Dircet Memory Access

Eight DMA channels are supported by the system. Two Intel 8237-5 DMA controller chips (four channels in each chip) are used to provide eight DMA channels. The DMA channels are assigned as follows:

CTR 1		CTR 2	
CH 0	Spare	CH 4	Cascade for CTRL 1
CH 1	SDLC	CH 5	Spare
CH 2	Diskette	CH 6	Spare
CH 3	Spare	CH 7	Spare

DMA Channel

Channels 0 through 3 are contained in DMA controller 1. Transfers of 8-bit data, 8-bit I/O adapters and 8-bit or 16-bit system memory are supported by these channels. Each of these channels will transfer in 64KB blocks throughout the 16-megabyte system address space.

Channels 4 through 7 are contained in DMA controller 2. To cascade channels 0 through 3 to the microprocessor, use channel 4. Transfers of 16-bit data between 16-bit adapters and 16-bit system memory are supported by channels 5, 6 and 7. DMA channels 5 through 7 will transfer data in 128KB blocks throughout the 16-megabyte system address space. These channels will not transfer data on odd-byte boundaries.

The addresses for the page register are as follows:

Page Register	I/O Hex Address
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

Address generation for the DMA channels is as follows:

For DMA Channels 3 through 0		
Source	DMA Page Registers	8237A - 5
Address	A23 ⟺ A16	A15 ⟺ A0

NOTE: To generate the addressing signal "byte high enable" (BHE), invert address line A0.

For DMA Channels 7 through 5		
Source	DMA Page Registers	8237A - 5
Address	A23 ⟺ A17	A16 ⟺ A1

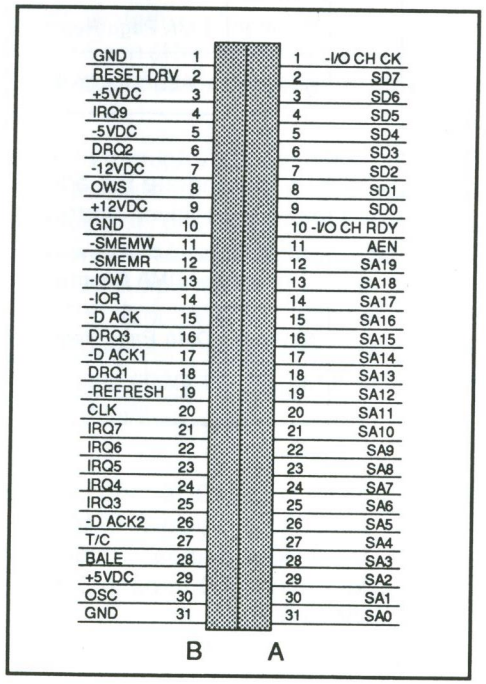
NOTE: The BHE and A0 addressing signals are forced to a logical 0. DMA channel addresses do not increase or decrease through page boundaries 64KB for channels 0 through 3 and 128KB for channels 5 through 7.

I/O Channel Slots

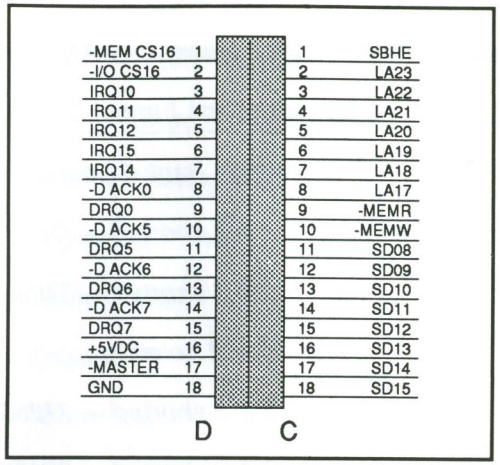
The I/O channel supports:

- Refresh of system memory from channel or microprocessors
- Selection of data accesses (either 8- or 16-bit)
- Interrupts
- 24-bit memory addresses (16MB)
- I/O wait-state generation.
- I/O address space hex 100 to hex 3FF.
- Open-bus structure (allowing multiple microprocessors to share the system's resources, including memory)
- DMA channels

The pinouts of the expansion bus I/O channels are shown as below and on the next page.



B		A	
GND	1	1	-I/O CH CK
RESET DRV	2	2	SD7
+5VDC	3	3	SD6
IRQ9	4	4	SD5
-5VDC	5	5	SD4
DRQ2	6	6	SD3
-12VDC	7	7	SD2
OWS	8	8	SD1
+12VDC	9	9	SD0
GND	10	10	-I/O CH RDY
-SMEMW	11	11	AEN
-SMEMR	12	12	SA19
-IOW	13	13	SA18
-IOR	14	14	SA17
-D ACK	15	15	SA16
DRQ3	16	16	SA15
-D ACK1	17	17	SA14
DRQ1	18	18	SA13
-REFRESH	19	19	SA12
CLK	20	20	SA11
IRQ7	21	21	SA10
IRQ6	22	22	SA9
IRQ5	23	23	SA8
IRQ4	24	24	SA7
IRQ3	25	25	SA6
-D ACK2	26	26	SA5
T/C	27	27	SA4
BALE	28	28	SA3
+5VDC	29	29	SA2
OSC	30	30	SA1
GND	31	31	SA0



D		C	
-MEM CS16	1	1	SBHE
-I/O CS16	2	2	LA23
IRQ10	3	3	LA22
IRQ11	4	4	LA21
IRQ12	5	5	LA20
IRQ15	6	6	LA19
IRQ14	7	7	LA18
-D ACK0	8	8	LA17
DRQ0	9	9	-MEMR
-D ACK5	10	10	-MEMW
DRQ5	11	11	SD08
-D ACK6	12	12	SD09
DRQ6	13	13	SD10
-D ACK7	14	14	SD11
DRQ7	15	15	SD12
+5VDC	16	16	SD13
-MASTER	17	17	SD14
GND	18	18	SD15

Math Coprocessor Control

The math coprocessor functions as an I/O device through I/O port addresses hex 0F8, 0FA and 0FC. The microprocessor sends OP codes and operands to I/O ports. The microprocessor also receives and stores results through the same I/O ports. The "busy" signal sent by the processor forces the microprocessor to wait until the coprocessor is finished executing.

The following describes the math coprocessor controls:

0F0

The latched math coprocessor busy signal can be cleared with an 8-bit "out" command to port F0. The coprocessor will latch "busy" if it asserts its error signal. Data output should be zero.

0F1

The math coprocessor will reset if an 8-bit "out" command is sent to port F1. Again, the data output should be zero.

Appendix A

Quick Reference for Jumper Settings

W1 - W6 — Bank Selection

1 & 2 shorted — One or two RAM banks

2 & 3 shorted — Three or four RAM banks

W7 — ROM Selection

1 & 2 shorted — 27256 chip selected

2 & 3 shorted — 27128 chip selected

W8 — Pipeline

1 & 2 shorted — Pipelining disable

2 & 3 shorted — Pipelining enable

W9 — 80387SX

1 & 2 shorted — Coprocessor enable

2 & 3 shorted — Coprecessor disable

W11 — Power Good Selection

1 & 2 shorted — Onboard

2 & 3 shorted — External

W12 — Display Mode

1 & 2 shorted — Mono

2 & 3 shorted — Color

W13 — Battery Selection

1 & 2 shorted — External

2 & 3 shorted — Onboard

J1 — CPU Frequency Indicator

J2 — Keylock & Power LED

J3 — Turbo Switch

J4 — Speaker

J5 — Turbo LED

J6 — Hardware Reset

J7 — External Battery Connector

J8 — Keyboard Connector

J9 — Power Connector